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ABSTRACT

The invention includes a method and apparatus for synchronizing a first processor with a second processor. The method includes storing in a register parallel bits of data from the first processor, wherein at least one bit of data is a logic ONE. An output signal is formed from the one bit of data in the register. The output signal is sent as an interrupt signal to an interrupt terminal of the second processor for synchronizing the first processor with the second processor. The method may be used with a memory mapped register or an off-core register. The first and second processors may each be a digital signal processor (DSP) or any other type of processor.

001210-25568100